MEMORY INTERFACE AND METHOD OF INTERFACING BETWEEN FUNCTIONAL ENTITIES

Abstract

A data and signal interface for controlling the transfer of data and signals between a memory array and macro function such as that of a digital signal processor (DSP) core. In one embodiment, the interface comprises a plurality of memory ports which interface with X/Y memory banks, a plurality of function ports, each with a function controller, which interface with DSP functions, a crossbar connecting the memory and function ports, and an arbitration unit for arbitrating memory access by the function ports. The memory interface advantageously allows multiple simultaneous accesses of memory banks via a plurality of macro functions, each access under the control of a parent processor instruction. A standardized protocol used for memory read/write operations is also disclosed.